IN THE SPECIFICATION

Please replace the paragraph beginning at page 7, line 3, as follows:

During operation of the circuit 50, s_{0c}, s_{1c}, s_{0c}, s_{03} are sequentially offered to the multiplication logic 60 . . . 63 on successive cycles by control means 99. At the outset of each column multiplication, the registers $MixCol_0$ to $MixCol_3$ are pre-set to zero.